QSFP+ Copper Cable Assembly

Overview

QSFP+ (Quad Small Form-factor Pluggable Plus) copper direct-attach cables are suitable for very short distances and offer a highly cost-effective way to establish a 40-Gigabit link between QSFP+ ports of QSFP+ switches within racks and across adjacent racks. These cables are used for 40GbE and Infniband standards, to maximize performance. QSFP+ are designed to meet emerging data center and high performance computing application needs for a high density cabling interconnect system capable of delivering an aggregate data bandwidth of 40Gb/s. This interconnect system is fully compliant with existing industry standard specifications such as the QSFP MSA and IBTA (InfiniBand Trade Association). The QSFP+ cables support the bandwidth transmission requirements as defined by IEEE 802.3ba (40 Gb/s) and Infiniband QDR (4x10 Gb/s per channel) specifications.



Features

- Compliant QSFP MSA specifications
- Fully compatible with IEEE802.3ba and Infiniband QDR specifications
- 40 Gb/s total bandwidth
- 4 independent duplex channels operating at 10Gbps, also support for 2.5Gbps, 5Gbps data rates
- 100 ohm differential impedance system
- Single 3.3V power supply, low power consumption, <1.5W
- Low Near-End Crosstalk(NEXT)
- Operating case temperature: -40 to 85°C
- All-metal housing for superior EMI performance
- Precision process control for minimization of pair-to-pair skew
- AC coupling of PECL signals
- EEPROM for cable signature & system communications
- 30 AWG to 24 AWG cable sizes available
- RoHS compliant

Applications

▶ Data

Servers
Networked storage systems
Routers
External storage systems

Data Center networking

▶ Communications

Switches Routers

► Industry Standards

InfiniBand Trade Association (IBTA)
IEEE802.3ba
40Gigabit Ethernet (40G BASE – CR4)

Absolute Maximum Ratings

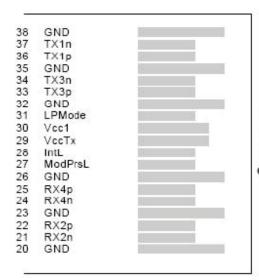
Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	Tst	-40	125	degC	
Relative Humidity (non-condensation)	RS	-	85	%	
Operating Case Temperature	Торс	-40	85	degC	1
Supply Voltage	VCC3	-0.3	3.6	V	
Voltage on LVTTL Input	Vilvttl	-0.3	VCC3 +0.2	V	

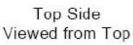
NOTE: Stress or conditions exceed the above range may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not applied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

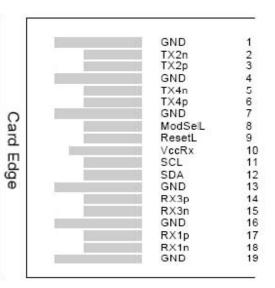
Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature	Торс	-40	85	degC
Relative Humidity (non-condensation)	RS	-	85	%
Supply Voltage	VCC3	3.135	3.465	V
Power Supply Currenct	ICC3	750	-	mA
Total Power Consumption	Pd	-	2.0	W

Pin Assignments and Descriptions







Bottom Side Viewed from Bottom

PIN	Logic	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1

5 CML-I Tx4n Transmitter Inverted Date 6 CML-I Tx4p Transmitter Non-Inverted ID 7 GND Ground 8 LVTLL-I ModSelL Module Select 9 LVTLL-I ResetL Module Reset 10 Vcc Rx + 3.3V Power Supply F 11 LVCMOS-I/O SCL 2-Wire Serial Interface 12 LVCMOS-I/O SDA 2-Wire Serial Interface 13 GND Ground 14 CML-O Rx3p Receiver Non-Inverted Date 15 CMLO Rx3n Receiver Inverted Date 16 GND Ground 17 CMLO Rx1p Receiver Inverted Date 18 CMLO Rx1n Receiver Inverted Date 19 GND Ground	
7 GND Ground 8 LVTLL-I ModSelL Module Select 9 LVTLL-I ResetL Module Reset 10 Vcc Rx + 3.3V Power Supply F 11 LVCMOS-I/O SCL 2-Wire Serial Interface 12 LVCMOS-I/O SDA 2-Wire Serial Interface 13 GND Ground 14 CML-O Rx3p Receiver Non-Inverted Data 15 CMLO Rx3n Receiver Inverted Data 16 GND Ground 17 CMLO Rx1p Receiver Non-Inverted Data 18 CMLO Rx1n Receiver Inverted Data	-
8 LVTLL-I ModSelL Module Select 9 LVTLL-I ResetL Module Reset 10 Vcc Rx + 3.3V Power Supply F 11 LVCMOS-I/O SCL 2-Wire Serial Interface 12 LVCMOS-I/O SDA 2-Wire Serial Interface 13 GND Ground 14 CML-O Rx3p Receiver Non-Inverted Data 15 CMLO Rx3n Receiver Inverted Data 16 GND Ground 17 CMLO Rx1p Receiver Non-Inverted Data 18 CMLO Rx1n Receiver Inverted Data	1
9 LVTLL-I ResetL Module Reset 10 Vcc Rx + 3.3V Power Supply F 11 LVCMOS-I/O SCL 2-Wire Serial Interface 12 LVCMOS-I/O SDA 2-Wire Serial Interface 13 GND Ground 14 CML-O Rx3p Receiver Non-Inverted Data 15 CMLO Rx3n Receiver Inverted Data 16 GND Ground 17 CMLO Rx1p Receiver Non-Inverted Data 18 CMLO Rx1n Receiver Inverted Data	
10 Vcc Rx + 3.3V Power Supply F 11 LVCMOS-I/ O SCL 2-Wire Serial Interface 12 LVCMOS-I/ O SDA 2-Wire Serial Interface 13 GND Ground 14 CML-O Rx3p Receiver Non-Inverted Data 15 CMLO Rx3n Receiver Inverted Data 16 GND Ground 17 CMLO Rx1p Receiver Non-Inverted Data 18 CMLO Rx1n Receiver Inverted Data	
11 LVCMOS-I/O SCL 2-Wire Serial Interface 12 LVCMOS-I/O SDA 2-Wire Serial Interface 13 GND Ground 14 CML-O Rx3p Receiver Non-Inverted Data 15 CMLO Rx3n Receiver Inverted Data 16 GND Ground 17 CMLO Rx1p Receiver Non-Inverted Data 18 CMLO Rx1n Receiver Inverted Data	
11 O SCL 2-Wire Serial Interface 12 LVCMOS-I/O SDA 2-Wire Serial Interface 13 GND Ground 14 CML-O Rx3p Receiver Non-Inverted Data 15 CMLO Rx3n Receiver Inverted Data 16 GND Ground 17 CMLO Rx1p Receiver Non-Inverted Data 18 CMLO Rx1n Receiver Inverted Data	Receiver 2
12 O SDA 2-Wire Serial Interface 13 GND Ground 14 CML-O Rx3p Receiver Non-Inverted Data 15 CMLO Rx3n Receiver Inverted Data 16 GND Ground 17 CMLO Rx1p Receiver Non-Inverted Data 18 CMLO Rx1n Receiver Inverted Data	: Clock
14 CML-O Rx3p Receiver Non-Inverted Data 15 CMLO Rx3n Receiver Inverted Data 16 GND Ground 17 CMLO Rx1p Receiver Non-Inverted Data 18 CMLO Rx1n Receiver Inverted Data	e Data
15 CMLO Rx3n Receiver Inverted Data 16 GND Ground 17 CMLO Rx1p Receiver Non-Inverted Data 18 CMLO Rx1n Receiver Inverted Data	
16 GND Ground 17 CMLO Rx1p Receiver Non-Inverted Data 18 CMLO Rx1n Receiver Inverted Data	ata Output
17 CMLO Rx1p Receiver Non-Inverted Data 18 CMLO Rx1n Receiver Inverted Data	Output
18 CMLO Rx1n Receiver Inverted Data	1
	ata Output
10 CND Cround	Output
I GIVD GIOUNG	1
20 GND Ground	1
21 CMLO Rx2n Receiver Inverted Data	Output
22 CMLO Rx2p Receiver Non-Inverted Da	ata Output
GND Ground	1
24 CMLO Rx4n Receiver Inverted Data	Output 1
25 CMLO Rx4p Receiver Non-Inverted Da	ata Output
26 GND Ground	1
27 LVTTLO ModPrsL Module Present	t
28 LVTTLO IntL Interrupt	
29 Vcc Tx +3.3 V Power Supply tra	ansmitter 2
30 Vcc1 +3.3 V Power Sup	ply 2
31 LVTTLI LPMode Low Power Mod	ν ν ν
32 GND Ground	· ·

33	CMLI	Тх3р	Transmitter Non-Inverted Data Input	
34	CMLI	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CMLI	Tx1p	Transmitter Non-Inverted Data Input	
37	CMLI	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

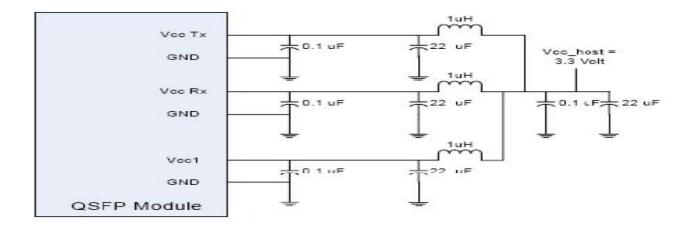
- 1. GND is the symbol for signal and supply (power) common for QSFP modules. All are common within the QSFP module and all module voltages are referenced to this potential otherwise noted. Connect these directly to the host board signal common ground plane.
- 2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

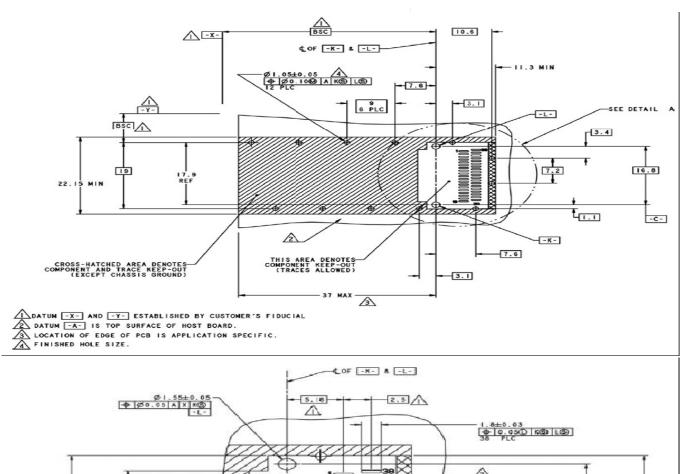
Recommended power supply filtering Example of QSFP Host board schematics.

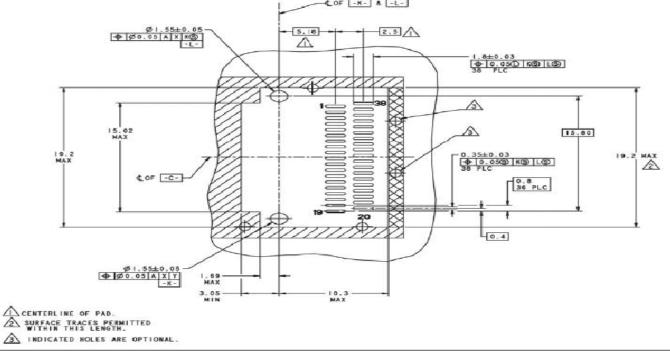
A typical host board mechanical layout for attaching the QSFP transceiver is presented below. The recommended host electrical connector should be a 38-pin IPASS right angle connector assembly (example: Tyco PN: 1761987-9) and the cage assembly should be QSFP single cage (example: Tyco PN: 1888617-1).

Recommended PCB layout

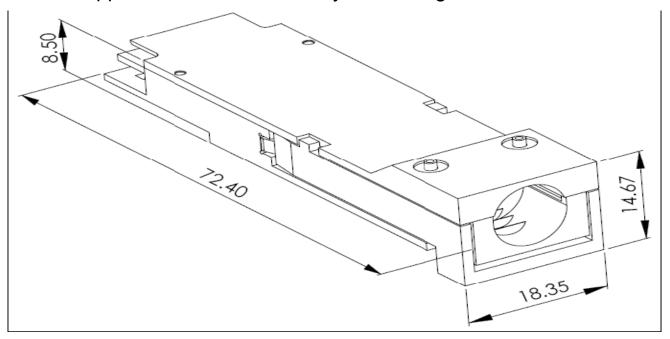
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QSFP Copper Module Outline for System Design



Mechanical Dimensions

